MAE140 - Linear Circuits - Winter 17 Final, March 21, 2017

Instructions

- (i) The exam is open book. You may use your class notes and textbook. You may use a hand calculator with no communication capabilities.
- (ii) You have 180 minutes
- (iii) Do not forget to write your name and student number
- (iv) On the questions for which the answers are given, please provide detailed derivations
- (v) The exam has 5 questions for a total of 50 points and 2 bonus points

Good luck!

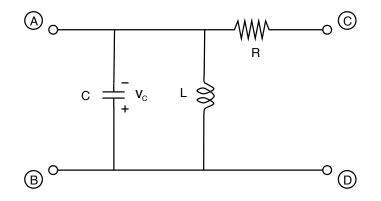


Figure 1: Circuit for Question 1.

1. Equivalent Circuits

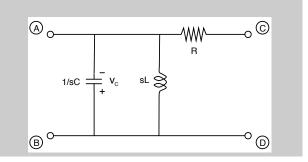
All impedances should be given as a ratio of two polynomials.

Part I: [1 point] Assuming zero initial conditions, transform the circuit in Figure 1 into the s-domain.

Solution:

Since all initial conditions are zero, it is easy to transform the circuit to the *s*-domain.

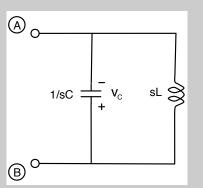
(1 point)



Part II: [2 points] For the circuit you obtained in Part I, find the equivalent impedance as seen from terminals (A) and (B).

Solution:

We redraw the circuit slightly to make it more clear how it looks from terminals (\widehat{A}) and (\widehat{B}) .



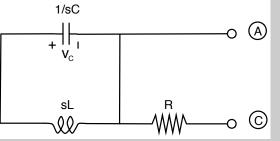
The resistor on the right plays no role because the circuit is open on the right. (1 point) The capacitor and the inductor are in parallel. Hence the equivalent impedance as seen from terminals (\widehat{A}) and (\widehat{C}) is

$$\frac{1}{sC} \| sL = \frac{sL}{s^2 LC + 1} \tag{1 point}$$

Part III: [2 points] For the circuit you obtained in Part I, find the equivalent impedance as seen from terminals (A) and (C).

Solution:

We redraw the circuit slightly to make it more clear how it looks from terminals (\widehat{A}) and (\widehat{C}) .

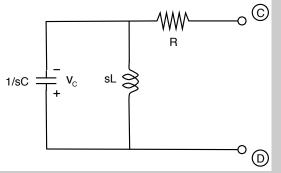


The capacitor and the inductor are in series, and their combination, sL + 1/sC is in parallel with a zero impedance, so the play no role. (1 point) Hence the equivalent impedance as seen from terminals (A) and (C) is R. (1 point)

Part IV: [2 points] For the circuit you obtained in Part I, find the equivalent impedance as seen from terminals (Ĉ) and (D).

Solution:

We redraw the circuit slightly to make it more clear how it looks from terminals $(\overline{\mathbb{C}})$ and $(\overline{\mathbb{D}})$.



The capacitor and the inductor are in parallel, and their combination is in series with the

resistor R.

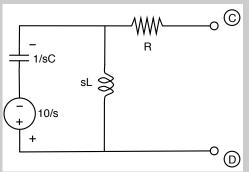
The equivalent impedance as seen from terminals $(\overline{\mathbb{C}})$ and $(\overline{\mathbb{D}})$ is

$$R + sL \| \frac{1}{sC} = R + \frac{sL/(sC)}{sL + \frac{1}{sC}} = R + \frac{sL}{s^2LC + 1} = \frac{RLCs^2 + sL + R}{s^2LC + 1}$$
(1 point)

Part V: [3 points] If the initial condition of the capacitor is instead $v_C(0) = 10V$, what is the *s*-domain Thévenin equivalent of the circuit as seen from terminals $(\widehat{\mathbb{C}})$ and $(\widehat{\mathbb{D}})$?

Solution:

If the initial condition of the capacitor is not zero, the circuit then looks like the plot on the right



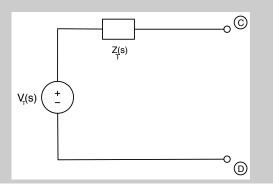
(1 point for correct initial condition)

We need to find V_T and Z_T . Since there are no dependent sources, we can compute Z_T by turning off the voltage source. This yields precisely the circuit we consider in Part III, and so the Thévenin impedance is

$$Z_T(s) = \frac{RLCs^2 + sL + R}{s^2LC + 1}$$
(1 point)

To compute V_T , we need to find the open-circuit voltage. The resistor R does not have any current going through it, hence it plays no role in the computation. The open circuit voltage is the one seen by the inductor. We can compute it by voltage division, taking good care of the sign,

$$V_T(s) = \frac{sL}{sL + 1/sC} \left(\frac{-10}{s}\right) = -\frac{10LCs}{s^2LC + 1}$$
(1 point)



The Thévenin equivalent circuit is the voltage source in series with the resistor

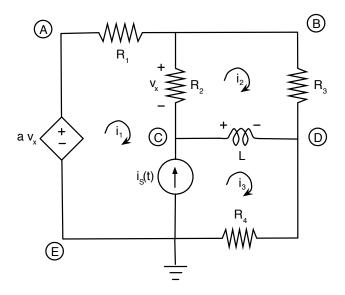
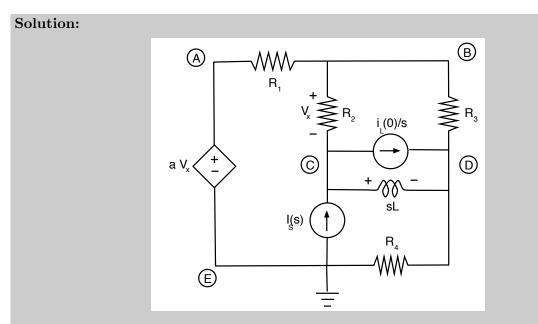


Figure 2: Nodal and Mesh Analysis Circuit for Question 2. a is a positive constant.

2. Nodal and Mesh Analysis

Part I: [5 points] Convert the circuit in Figure 2 to the *s*-domain and formulate its node-voltage equations. Use the reference node and other labels as shown in the figure. Do not assume zero initial conditions. Make sure your final answer has the *same* number of independent equations as unknown variables (notice the presence of the dependent source). No need to solve any equations!



In the above figure, we have transformed the circuit into the *s*-domain, taking good care of respecting the polarity of the inductor. Since we are going to use nodal analysis, we have taken care of the initial condition of the inductor using a current source.

(.5 point for correct circuit; .5 point for correct initial condition)

For nodal analysis, the presence of the voltage source poses a problem. However, the choice of ground provides a solution for it. In fact, we have $V_E = 0$ and

$$V_A(s) = aV_x(s) \tag{.75 point}$$

(this is method #2).

We next write KCL node equations for nodes (B), (C), and (D). For convenience, we use the shorthand notation $G_i = 1/R_i$. For node (B), we have

$$G_1(V_B(s) - V_A(s)) + G_2(V_B(s) - V_C(s)) + G_3(V_B(s) - V_D(s)) = 0$$
 (.75 point)

For node $(\widehat{\mathbf{C}})$, we have

$$G_2(V_C(s) - V_B(s)) + \frac{1}{sL}(V_C(s) - V_D(s)) = I_S(s) - i_L(0)/s$$
 (.75 point)

For node (\overline{D}) , we have

$$G_3(V_D(s) - V_B(s)) + G_4 V_D(s) + \frac{1}{sL}(V_D(s) - V_C(s)) = i_L(0)/s$$
 (.75 point)

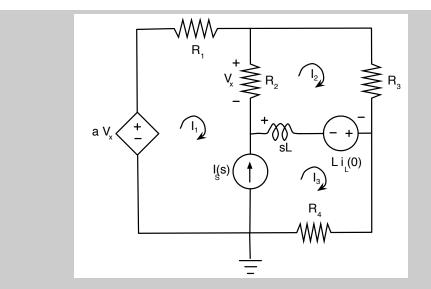
Finally, we take care of the dependent source by realizing that

$$V_x(s) = V_B(s) - V_C(s)$$
(1 point)

This gives a total of 5 independent equations in 5 unknowns $(V_A(s), V_B(s), V_C(s), V_D(s), V_x(s))$. Alternatively, one can take the expression for $V_x(s)$ and substitute it in the other equations to arrive at 4 independent equations in 4 unknowns $(V_A(s), V_B(s), V_C(s), V_D(s))$.

Part II: [5 points] Convert the circuit in Figure 2 to the *s*-domain and formulate its mesh-current equations. Use the mesh currents shown in the figure. Do not assume zero initial conditions. Make sure your final answer has the *same* number of independent equations as unknown variables (notice the presence of the dependent source). No need to solve any equations!

Solution:



In the above figure, we have transformed the circuit into the *s*-domain, taking good care of respecting the polarity of the inductor. Since we are going to use mesh current analysis, we have taken care of the initial condition of the inductor using a voltage source.

(.5 point for correct circuit; .5 point for correct initial condition) For mesh-current analysis, the presence of the current source is a problem that must be dealt with. In this case, we need to use a supermesh (because the current source is not in parallel with an impedance and because it belongs to more than one mesh). Therefore, we set

$$I_3(s) - I_1(s) = I_S(s) \tag{1 point}$$

(this is method #3).

KVL for the supermesh looks like

$$R_1I_1(s) + R_2(I_1(s) - I_2(s)) + sL(I_3(s) - I_2(s)) - Li_L(0) + R_4I_3(s) - aV_x(s) = 0 \quad (1 \text{ point})$$

For mesh 2, KVL takes the form

$$R_2(I_2(s) - I_1(s)) + R_3I_2(s) + Li_L(0) + sL(I_2(s) - I_3(s)) = 0$$
 (1 point)

Finally, we take care of the dependent source by realizing that

$$V_x(s) = R_2(I_1(s) - I_2(s))$$
 (1 point)

This gives a total of 4 independent equations in 4 unknowns $(I_1(s), I_2(s), I_3(s), V_x(s))$. Alternatively, one can take the expression for $V_x(s)$ and substitute it in the other equations to arrive at 3 independent equations in 3 unknowns $(I_1(s), I_2(s), I_3(s))$.

Part III: [1 bonus point] Express the transform of the inductor voltage using your unknown variables of Part I. Also, express the transform of the inductor voltage using your unknown variables of Part II.

Solution: We just need to be careful to not lose track of the transform of the inductor voltage. In the case of Part I, because we use a current source to account for the initial condition, we have

$$V_L(s) = V_C(s) - V_D(s)$$
 (.5 bonus point)

In the case of Part II, because we use a voltage source to account for the initial condition, we actually have

$$V_L(s) = sL(I_3(s) - I_2(s)) - Li_L(0)$$
 (.5 bonus point)

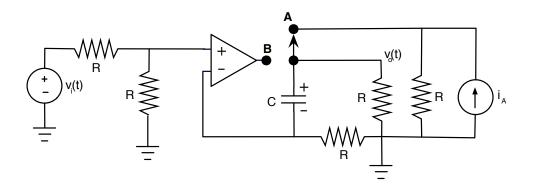


Figure 3: RCL circuit for Laplace Analysis for Question 3.

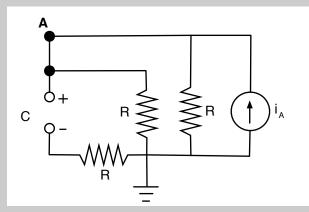
3. Laplace Domain Circuit Analysis

Part I: [2 points] Consider the circuit depicted in Figure 3. The value i_A of the current source at the right is constant. The switch is kept in position **A** for a very long time. At t = 0, it is moved to position **B**. Show that the initial condition for the capacitor is given by

$$v_C(0^-) = \frac{R}{2}i_A.$$

[Show your work]

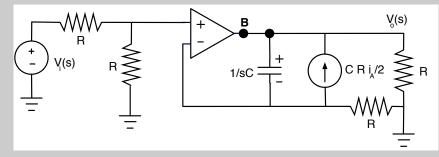
Solution: To find the initial condition, we substitute the capacitor by an open circuit. [1 point for correct circuit; 1 point for substituting capacitor by open circuit]



Therefore, using current division, we deduce that

$$v_C(0^-) = \frac{R}{2}i_A$$

Part II: [4 points] Use this initial condition to transform the circuit into the s-domain for $t \ge 0$. Use an equivalent model for the capacitor in which the initial condition appears as a current source. Use nodal analysis to express the output response transform $V_o(s)$ as a function of $V_i(s)$ and i_A . **Solution:** As instructed, we add one current source in parallel for the capacitor to take care of its initial condition, paying special attention to the direction of the current.



(.5 point for correct circuit; .5 point for correct current direction)

We do not recognize this circuit as any of the basic op-amp building blocks, so we use node analysis. Because we deal with ideal op-amps, we have

$$V_n(s) = V_p(s) = \frac{V_i(s)}{2}$$
(1 point)

The remaining KCL equation is

$$sC(V_n(s) - V_o(s)) + \frac{1}{R}V_n(s) + \frac{1}{2}CRi_A = 0$$
 (1 point)

Solving for $V_o(s)$, we obtain the output response transform

$$V_o(s) = \frac{1}{sC} \left(\left(\frac{1}{R} + sC \right) V_n(s) + \frac{1}{2} CRi_A \right)$$

= $\frac{1}{2} \left(\frac{1 + RCs}{RCs} V_i(s) + \frac{R}{s} i_A \right)$ (1 point)

Part III: [2 points] Use partial fractions and inverse Laplace transforms to show that the output voltage $v_o(t)$ when $i_A = 2 m A$, $v_i(t) = 12e^{-t}u(t) V$, C = 6 m F, and $R = 1 \text{ K}\Omega$ is

$$v_o(t) = (5e^{-t} + 2)u(t).$$

Solution: From our answer to Part II, and substituting the values for the impedances and the sources, the Laplace transform of the output voltage is (after some simplifications)

$$V_o(s) = \frac{1+6s}{s} \frac{1}{s+1} + \frac{1}{s}$$
(1 point)

Using partial fractions, we get

$$V_o(s) = \frac{A}{s} + \frac{B}{s+1} + \frac{1}{s}$$
 (.5 point)

Using the residue method to compute A and B, we obtain

$$V_o(s) = \frac{1}{s} + \frac{5}{s+1} + \frac{1}{s} = \frac{5}{s+1} + \frac{2}{s}$$
(.5 point)

The output voltage is then

$$v_o(t) = (5e^{-t} + 2)u(t)$$

Part IV: [2 points] Decompose the output voltage of Part III as (i) the sum of the natural and forced response, and (ii) the sum of the zero-state and zero-input response.

Solution: The forced response is the part of the output transform that has the same poles as the input. The pole of the input is at -1, therefore according to our derivations in Part III, we have

$$v_{o,fr}(t) = 5e^{-t}u(t) \tag{.5 point}$$

The remaining is the natural response

$$v_{o,nr}(t) = 2u(t) \tag{.5 point}$$

The zero-input response is what we obtained when the input is set to zero, hence

1

$$v_{o,zi}(t) = u(t) \tag{.5 point}$$

The zero-state response is what we obtained when the initial conditions are set to zero, hence

$$v_{o,zi}(t) = (5e^{-t} + 1)u(t)$$
 (.5 point)

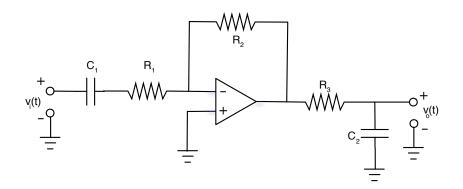
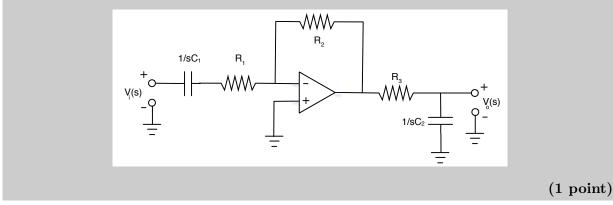


Figure 4: Frequency Response Analysis for Question 4.

4. Frequency Response Analysis

Part I: [1 point] Assuming zero initial conditions, transform the circuit in Figure 4 into the s-domain.

Solution: Since all initial conditions are zero, there is no need to add an independent source for the capacitors. Therefore, the circuit in the *s*-domain looks like



Part II: [2 points] Show that the transfer function from $V_i(s)$ to $V_o(s)$ is given by

$$T(s) = \frac{V_o(s)}{V_i(s)} = -\frac{R_2C_1s}{(R_1C_1s + 1)(R_3C_2s + 1)}$$

[Show your work]

Solution: This circuit is the combination of an inverting op-amp and a voltage divider. The chain rule holds because the voltage divider is connected to the output of an op-amp, which has zero output impedance. Therefore, the transfer function is the product of the two transfer functions of the individual stages. (1 point)

The transfer function for the inverting op-amp is

$$T_1(s) = -\frac{R_2}{R_1 + 1/sC_1} = -\frac{R_2C_1s}{R_1C_1s + 1}$$
 (.5 point)

The transfer function for the voltage divider is

$$T_2(s) = \frac{1/sC_2}{R_3 + 1/sC_2} = \frac{1}{R_3C_2s + 1}$$
 (.5 point)

Their product corresponds to the transfer function T(s) in the statement of Part II.

Part III [5.5 points] Let $R_1 = R_2 = R_3 = 1 \text{ K}\Omega$, $C_1 = 100 \,\mu\text{F}$ and $C_2 = 10 \,\mu\text{F}$. Compute the gain and phase functions of T(s). What are the DC gain and the ∞ -freq gain? What are the corresponding values of the phase function? What are the cut-off frequencies? Sketch plots for the gain and phase functions. What type of filter is this one? [Explain your answer]

Solution: For the given values of resistors and capacitors, the transfer function takes the form

$$T(s) = T_1(s)T_2(s) = -\frac{s}{s+10}\frac{100}{s+100} = -\frac{100s}{(s+10)(s+100)}$$

This is the product of a first-order high-pass filter and a first-order low-pass filter. The frequency response is then the complex function

$$T(j\omega) = T_1(j\omega)T_2(j\omega) = -\frac{j\omega}{j\omega+10}\frac{100}{j\omega+100}, \quad \omega \ge 0$$

Its magnitude is the gain function,

$$|T(j\omega)| = |T_1(j\omega)||T_2(j\omega)| = \frac{\omega}{\sqrt{\omega^2 + 100}} \frac{100}{\sqrt{\omega^2 + 10000}} = \frac{100\omega}{\sqrt{(\omega^2 + 100)(\omega^2 + 10000)}}$$
(.5 point)

The phase function is

$$\angle T(j\omega) = \angle (-j\omega) + \angle (100) - \angle (j\omega + 10) - \angle (j\omega + 100)$$
$$= \frac{3\pi}{2} + 0 - \arctan\left(\frac{\omega}{10}\right) - \arctan\left(\frac{\omega}{100}\right) \text{ rad} \qquad (.5 \text{ point})$$

At $\omega = 0$, we obtain

$$|T(j0)| = 0, \quad \angle T(j0) = \frac{3\pi}{2}$$
 rad

(correct DC-gain gets .5 point, correct phase gets .5 point)

At $\omega = 0$, we obtain

$$|T(j\infty)| = 0$$
, $\angle T(j\infty) = \frac{\pi}{2}$ rad
(correct ∞ -freq gain gets .5 point, correct phase gets .5 point)

This is not surprising, since we know from class that a high-pass filter and low-pass filter in series, with their cut-off frequencies properly chosen, give rise to a bandpass filter, which is what these DC- and ∞ -gains seem to point to.

Let's figure out what the cut-off frequencies are. For the high-pass filter, we have

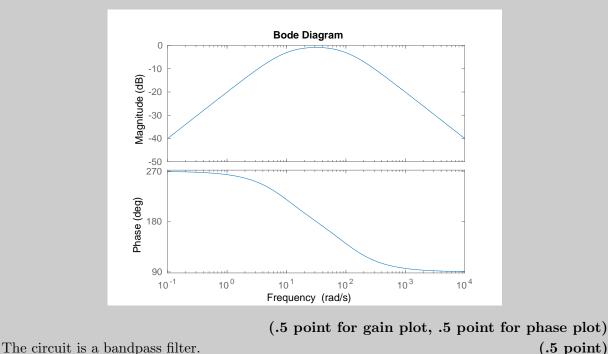
$$\omega_{c1} = 10 \text{ rad/s} \tag{.5 point}$$

For the low-pass filter, we have

$$\omega_{c2} = 100 \text{ rad/s} \tag{.5 point}$$

In fact, for ω very small, the gain function can be approximated by $\omega/10$. For very large values of ω , the gain function can be approximated by $100/\omega$. And for values between ω_{c1} and ω_{c2} , the gain function can be approximated by 1. The intersection of these asymptotes also yields the two cut-off frequencies above.

With the values obtained above, you can sketch the magnitude of the frequency response as



Part IV [1.5 points] Using what you know about frequency response, compute the steady state response $v_o^{SS}(t)$ of this circuit when $v_i(t) = \cos(50t + \frac{\pi}{4})$ using the same values of R_1, R_2, R_3, C_1 , and C_2 as in Part III.

Solution: To compute the steady-state response to the input $v_i(t) = \cos(50t + \frac{\pi}{4})$, we use the frequency response values for $\omega = 50$,

(.5 point)

$$|T(j50)| \simeq 0.877058$$

 $\angle T(j50) = \frac{3\pi}{2} - \arctan(5) - \arctan(\frac{1}{2}) \simeq 2.87534 \text{ rad.}$

Therefore,

$$v_o^{SS}(t) = |T(j50)| \cos\left(50t + \frac{\pi}{4} + \angle T(j50)\right)$$
(1 point for correct expression)
= 0.877058 cos (50t + 3.66074)
(.5 point for correct values)

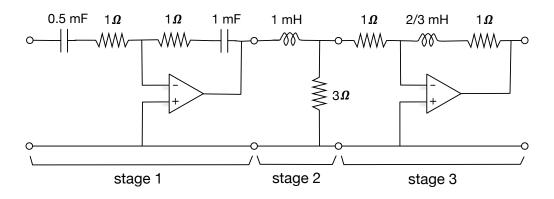


Figure 5: Circuit for Question 5.

5. Loading and the Chain Rule

A former instructor of MAE140 was given the task of designing a circuit with the following transfer function

$$T(s) = \frac{2s^2 + 5000s + 3 \cdot 10^6}{s^2 + 5000s + 6 \cdot 10^6}$$

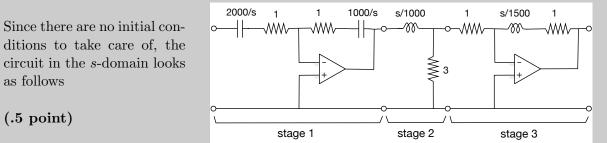
He decomposed the transfer function as follows

$$T(s) = \left(-\frac{s+1000}{s+2000}\right) \left(\frac{3000}{3000+s}\right) \left(-\frac{s+1500}{1500}\right)$$

and came up with the design in Figure 5.

Part I: [2 points] Consider each stage in Figure 5 separately, and compute the transfer function of each one. Show that the product of the 3 transfer functions is equal to T(s).

Solution:



Stage 1 and 3 are inverting op-amps, and stage 2 is a voltage divider. The transfer function of stage 1 is

$$T_1(s) = -\frac{1+1000/s}{1+2000/s} = -\frac{s+1000}{s+2000}$$
(.5 point)

The transfer function of stage 2 is

$$T_2(s) = \frac{3}{3 + s/1000} = \frac{3000}{3000 + s}$$
(.5 point)

The transfer function of stage 3 is

$$T_3(s) = -\frac{1+s/1500}{1} = -\frac{s+1500}{1500}$$
(.5 point)

It is clear that their product is equal to T(s)

Part II: [1 point] In spite of Part I, explain why the circuit designed by the instructor is not a valid solution. Properly justify your answer.

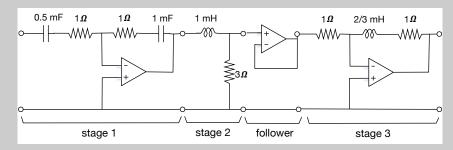
Solution: The circuit is not a valid solution because there is loading. Stage 2 does not load stage 1 because is directly connected to the first op-amp, and the output impedance of an ideal op-amp is zero. However, stage 3 is loading stage 2, because there is current going through the 1Ω resistor. (1 point)

Part III: [1 point] Could you fix the design provided by the instructor by re-ordering the stages without modifying anything else? Again, justify your answer.

Solution: Yes! We can swap stages 3 and 2 (to create a stage1-stage3-stage2 configuration). That would resolve the loading. In the new configuration, stage 3 does not load stage 1 because of the zero output impedance of the op-amp. The same reason makes sure that stage 2 does not load stage 3. Consequently the overall transfer function is the product of the individual transfer functions, which is T(s). (1 point)

Part IV: [1 point] Could you fix the design provided by the instructor by using one more op-amp without re-ordering the stages?

Solution: Yes again! Without reordering the stages, we could add a voltage follower between stages 2 and 3 to fix the loading in the design of Figure 5, as shown in the following plot



The voltage follower has infinite input impedance and zero output impedance, making sure, respectively, that it does not load stage 2 and is not loaded by stage 3. (1 point)

Part V: [5 points] Provide an alternative design solution that only uses 1 op-amp and components with the same values as those used in the instructor's design (i.e., 1Ω -resistors, 1 mH- and 2/3 mH- inductors, and 0.5 mF- and 1 mF-capacitors). Your design should be based on connecting two voltage dividers and one non-inverting op-amp. Make sure you properly justify that the chain rule applies.

Solution: Our alternative design is based on the following decomposition of the transfer function T(s) as a product of fractions of polynomials,

$$T(s) = \left(\frac{s+1000}{s+2000}\right) 2\left(\frac{s+1500}{s+3000}\right)$$

We can make this happen with two voltage dividers (with transfer functions $\frac{s+1000}{s+2000}$ and $\frac{s+1500}{s+3000}$) and one non-inverting op-amp with gain 2. (1 point)

The voltage divider on the right has transfer function

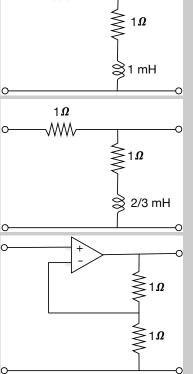
$$\frac{s+1000}{s+2000}$$

(1 point for design)

The voltage divider on the right has transfer function

$$\frac{s+1500}{s+3000}$$

(1 point for design)



1Ω

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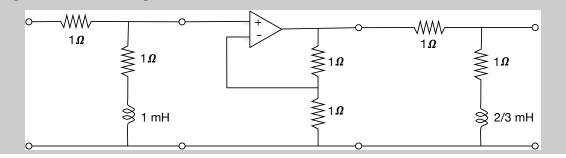
The non-inverting op-amp on the right has transfer function

 $\mathbf{2}$

(1 point for design)

If we put the three circuits together, with the non-inverting op-amp in between the voltage dividers, we make sure no loading arises (having the op-amp as the first or the last stage would result in loading). (1 point)

This gives rise to the design



Part VI: [1 bonus point] Name (i) one criteria for which your design in Part IV is better than your design in Part V, and (ii) one criteria for which your design in Part V is better than your design in Part VI.

Solution: For (i), output impedance. Our design in Part IV as zero-output impedance, which means that we can connect anything as a load and the output voltage will not change. That is not the case with our design in Part V. (.5 point) For (ii), number of components. Our design in Part V uses less components than our design in Part IV (including only 1 op-amp versus 3 op-amps). (.5 point)