MAE40 - Linear Circuits - Fall 20
Final Exam, December 19, 2020

Instructions

(i) Prior to the exam, you must have completed the Academic Integrity Pledge at `https://academicintegrity.ucsd.edu/forms/form-pledge.html`

(ii) The exam is open book. You may use your class notes and textbook

(iii) Collaboration is not permitted. The answers you provide should be the result only of your own work

(iv) On the questions for which the answers are given, please provide detailed derivations

(v) The exam has 4 questions for a total of 40 points and 2 bonus points

(vi) You have from 8:00am to 11:00am to complete the exam. Allow sufficient time to post your answers in Canvas (submission closes at 11:15am).

(vii) If there is any clarification needed, post your question in the "Discussions" tab of the class Canvas webpage ("Clarifications on question statements of final")

Good luck!

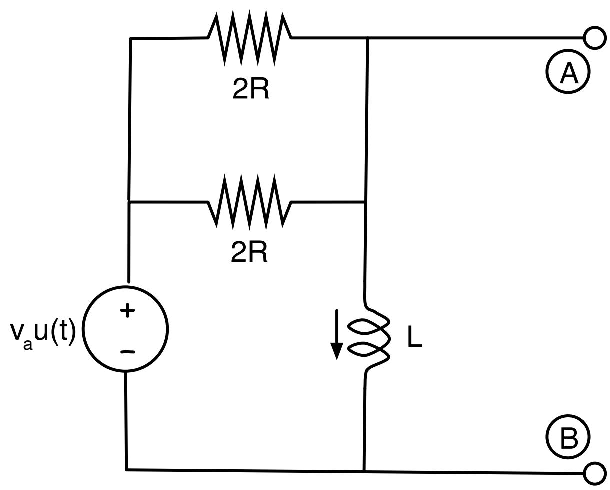

Figure 1: Circuit for Question 1.

1. **Equivalent Circuits**

Here, v_a is a constant.

Part I: [2 points] Assuming $i_L(0) = 1A$, transform the circuit in Figure 1 into the s-domain, using a voltage source to account for the initial condition of the inductor.

Part II: [2 points] For the circuit you obtained in Part I, find the open-circuit voltage transform as seen from terminals A-B. The answer should be given as a ratio of two polynomials.

Part III: [2 points] For the circuit you obtained in Part I, find the short-circuit current transform as seen from terminals A-B. The answer should be given as a ratio of two polynomials.

Part IV: [2 points] For the circuit you obtained in Part I, find the Thévenin equivalent in the s-domain as seen from terminals A-B (the impedance should be given as a ratio of two polynomials).

Part V: [2 points] Break down the open-circuit voltage transform you obtained in Part II as the sum of the zero-state and zero-input response transforms. Do the same as the sum of the forced and natural response transforms.

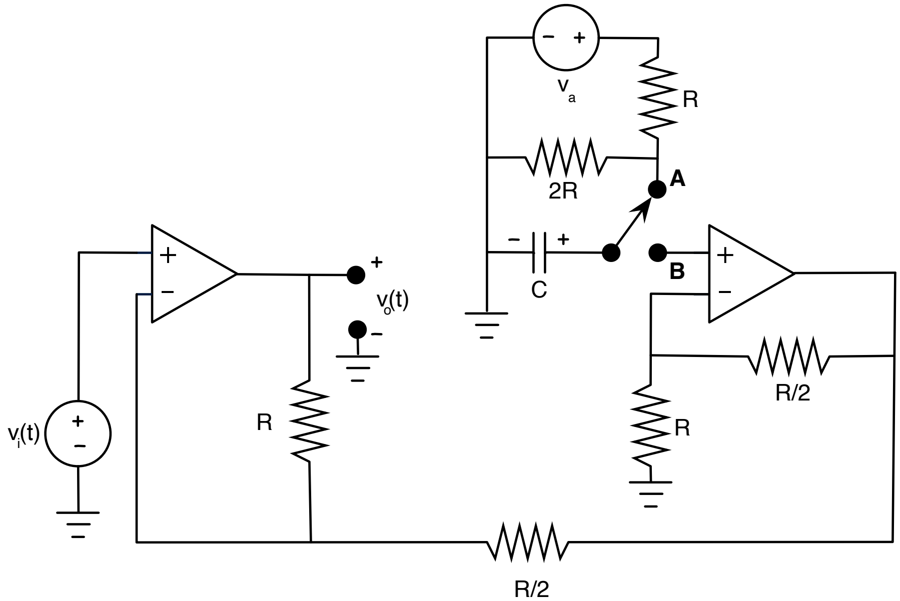

Figure 2: RCL circuit for Laplace Analysis for Question 2.

2. **Laplace Domain Circuit Analysis**

Part I: [2 points] Consider the circuit depicted in Figure 2. The value v_a of the current source is constant. The switch is kept in position **A** for a very long time. At $t = 0$, it is moved to position **B**. Show that the initial condition for the capacitor is given by

$$v_C(0^-) = \frac{2}{3}v_a.$$

[Show your work]

Part II: [5 points] Use this initial condition to transform the circuit into the s-domain for $t \geq 0$. Use an equivalent model for the capacitor in which the initial condition appears as a voltage source. Use nodal analysis to express the output response transform $V_o(s)$ as a function of $V_i(s)$ and v_a.

Part III: [3 points] Use partial fractions and inverse Laplace transforms to show that the output voltage $v_o(t)$ when $v_a = 2\,\mathrm{V}$, $v_i(t) = te^{-2t}u(t)\,V$, $C = 10\,m\mathrm{F}$, and $R = 100\,K\Omega$ is

$$v_o(t) = \big(3te^{-2t} - 4\big)u(t).$$

Part IV: [Extra 2 points] Decompose the output voltage of Part III as (i) the sum of the natural and forced response, and (ii) the sum of the zero-state and zero-input response.

3. **Frequency Response Analysis**

Consider the transfer function

$$T(s) = \frac{500s}{s^2 + 520s + 10^4}$$

Part I [3 points] Compute the gain $|T(j\omega)|$ and phase $< T(j\omega)$ functions

Part II [3 points] What are the DC gain and the ∞-freq gain? What are the corresponding values of the phase function? What are the cut-off frequencies?

Part III [2 points] Sketch plots for the gain and phase functions. What type of filter is this one? [Explain your answer]

Part IV [2 points] Using what you know about frequency response, compute the steady-state response $v_o^{SS}(t)$ to the input $v_i(t) = \cos(300t + \frac{\pi}{4})$.

4. **OpAmp Design**

Consider the transfer function

$$T(s) = \frac{500s}{s^2 + 520s + 10^4}$$

of the previous question.

Part I: [4 points] Consider the following factorization of the transfer function

$$T(s) = \frac{-20}{s+20} \cdot \frac{-25s}{s+500}$$

Based on this decomposition, design a circuit as the series connection of two stages, each with 1 OpAmp, that implements $T(s)$. Additionally, you can only use 100Ω and 1KΩ-resistors, and $20\mu F$ and $50\mu F$-capacitors, and no inductors. Be sure to properly justify why the overall transfer function of your design is the product of the individual transfer function of each stage.

Part II: [3 points] Consider instead the following factorization of the transfer function

$$T(s) = \frac{s}{s+20} \cdot \frac{500}{s+500}$$

Based on this decomposition, design a circuit as the series connection of three stages, one with 1 OpAmp and the others without, that implements $T(s)$. Additionally, you can only use 100Ω and 1KΩ-resistors, and $20\mu F$ and $50\mu F$-capacitors, and no inductors. Be sure to properly justify why the overall transfer function of your design is the product of the individual transfer function of each stage.

Part III: [3 points] Finally, consider the following factorization of the transfer function

$$T(s) = \frac{20}{s+20} \cdot 25 \cdot \frac{s}{s+500}$$

Based on this decomposition, design a circuit as the series connection of three stages, one with 1 OpAmp and the others without, that implements $T(s)$. Additionally, you can only use 100Ω and 1KΩ-resistors, and $20\mu F$ and $50\mu F$-capacitors, and no inductors. Be sure to properly justify why the overall transfer function of your design is the product of the individual transfer function of each stage.