MAE40 - Linear Circuits - Fall 23 - Section A00
Final Exam, December 13, 2023

Instructions

(i) The exam is open book. You may use your class notes and textbook.
(ii) The exam has 4 questions for a total of 40 points and 4 bonus points.
(iii) You have from 11:30am to 2:30pm to do the exam – but should require less time!
(iv) You can use a calculator with no communication capabilities.
(v) In your responses, clearly *articulate your reasoning* and *properly justify the steps.*
(vi) **Important:** start each part below on a separate page, use only one side, and write your name & PID at the top of each page.

Good luck!

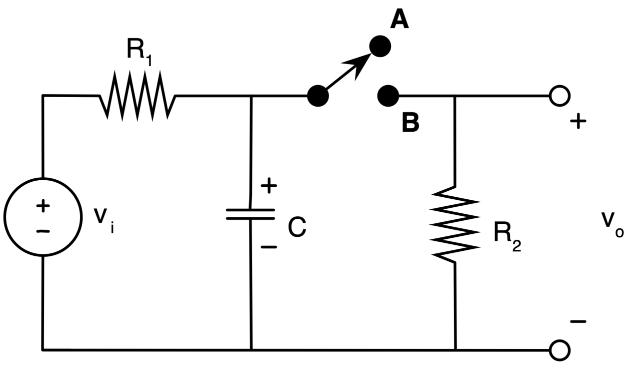

Figure 1: Circuit for Question 1.

1. **Equivalent Circuits**

Consider the circuit depicted in Figure 1. The value v_i of the voltage source is constant. The switch is kept in position **A** for a very long time. At time $t = 0$, it is moved to position **B**.

Part I: [2 points] Find the initial condition $v_C(0)$ for the capacitor.

Part II: [2 points] Transform the circuit in Figure 1 into the s-domain, using a current source to account for the initial condition of the capacitor.

Part III: [2 points] For the circuit you obtained in Part II, find the voltage transform $V_o(s)$. The answer should be given as a ratio of two polynomials.

Part IV: [2 points] What are the zero-state and zero-input components of $V_o(s)$?

Part IV: [2 points] What are the forced and natural components of $V_o(s)$?

2. **Laplace Domain Circuit Analysis**

Part I: [1 point] Consider the circuit depicted in Figure 2. The value i_a of the current source is constant. The switch is kept in position **A** for a very long time. At time $t = 0$, it is moved to position **B**. Find the initial condition for the inductor.

Part II: [2 points] Use this initial condition to transform the circuit into the s-domain for $t \geq 0$. Use an equivalent model for the inductor in which the initial condition appears as a voltage source.

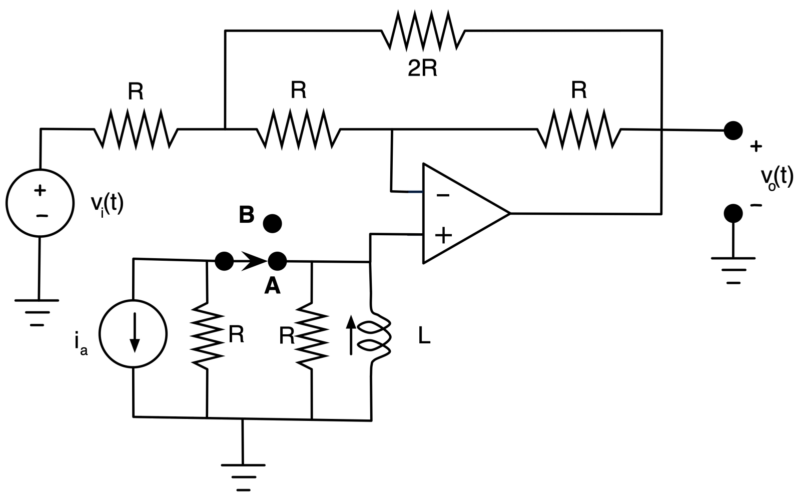

Figure 2: RL circuit for Laplace Analysis for Question 2.

Part III: [5 points] Use nodal analysis to show that the output response transform $V_o(s)$ as a function of $V_i(s)$ and i_a is expressed as

$$V_o(s) = -\frac{1}{3}V_i(s) + \frac{4}{3}\frac{RLi_a}{R + sL}$$

Part IV: [2 points] Use inverse Laplace transforms to show that the output voltage $v_o(t)$ when $v_i(t) = (1 - e^{-t})u(t)\,V$, $L = 1\,\text{mH}$, $i_a = 10\,\text{m}A$, and $R = 100\,\Omega$ is

$$v_o(t) = -\frac{1}{3}\big(1 - e^{-t} - 4e^{10^5 t}\big)u(t).$$

3. **Frequency Response Analysis**

An engineer measured the sensor signal

$$v_m(t) = \underbrace{\frac{1}{3}\cos\left(\frac{t}{6} - \pi\right)}_{\text{bias}} + \cos(2t) + \underbrace{\frac{1}{4}\cos\left(30t + \frac{\pi}{3}\right)}_{\text{noise}}$$

The first component corresponds to a time-varying bias, the second is the signal the engineer was actually interested in, and the third component corresponds to sensor noise. The engineer wanted to clean up the signal $v_m(t)$ to retrieve more clearly the component of interest. In order to do this, the engineer filtered the signal using the transfer function

$$T(s) = \frac{10s}{s^2 + 11s + 10}$$

In this problem, you will decide whether this was a reasonable choice. Do the following:

Part I [2 points] Compute the gain function $|T(j\omega)|$ and the phase function $< T(j\omega)$

Part II [4 points] What are the DC gain and the ∞-freq gain? What are the corresponding values of the phase function? What are the cut-off frequencies?

Part III [2 points] Sketch plots for the gain and phase functions. What type of filter is this one? [Explain your answer]

Part IV [2 points] Using what you know about frequency response, compute the steady-state response $v_o^{SS}(t)$ to the input $v_m(t)$. Did the transfer function selected by the engineer accomplish its goal? [Justify your answer]

4. **Circuit Design and Chain Rule**

In this question, you seek to design a circuit that implements the transfer function

$$T(s) = \frac{10s}{s^2 + 11s + 10}$$

used by the engineer in Question 3 to filter the sensor signal.

Part I: [2 points] Decompose $T(s)$ as a product $T_1(s) \cdot T_2(s)$ of two transfer functions $T_1(s), T_2(s)$ of the form

$$T_1(s) = \frac{s}{s + \alpha_1}, \quad T_2(s) = \frac{\alpha_2}{s + \alpha_2},$$

with $\alpha_1 < \alpha_2$.

Part II: [4 points] Design a voltage divider that implements the transfer function $T_1(s)$ and another voltage divider that implements the transfer function $T_2(s)$. You can use only capacitors and resistors, but no inductors. Allowable capacitor values are $10\,\mu$F, $100\,\mu$F, and resistors should be $10\,\text{K}\Omega$.

Part III: [2 points] Based on the decomposition in Part I and the designs in Part II, the engineer connected in series the two voltage dividers, but was surprised to see that, after filtering the sensor signal $v_m(t)$, the output was not the same as what you computed in Question 3, Part IV. Explain why.

Part IV: [2 points] How would you fix the design of the engineer in Part III so that the output of the filtered signal is indeed the same as what you computed in Question 3, Part IV? In your design, you can use up to one Op-Amp. Justify your design properly.

5. **Brief question for extra points (1/2)**

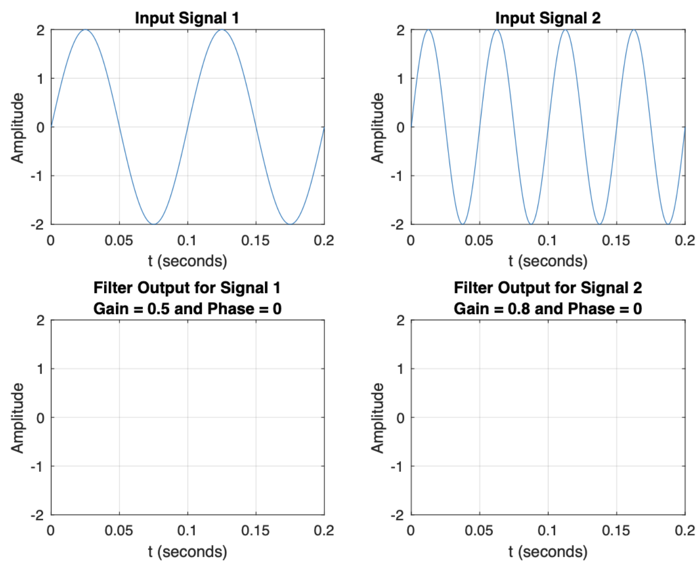

Figure 3: Signals for Question 5.

Figure 3 shows 2 input waveforms that go into a filter.

Part I: [Extra 1 point] Freehand sketch the filter's steady state output waveform in the time domain using the gain and phase shift shown in the title of the plots. Use the grid lines to draw the output waveform.

Part II [Extra 1 point] Is the filter a low-pass filter? Could it be a high-pass filter?

6. **Brief question for extra points (2/2)**

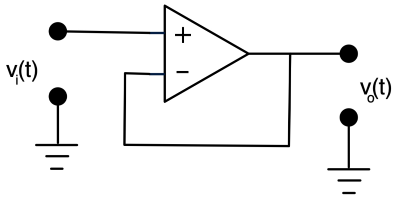

Figure 4: Circuit for Question 6.

For Op-Amp circuit shown in Figure 4, answer the questions below

Part I: [Extra 1 point] Calculate v_o as a function of v_i.

Part II [Extra 1 point] Explain why someone would use the above circuit in-between two stages instead of just directly connecting the two stages.

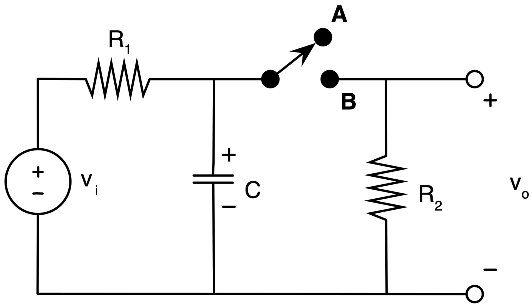

Figure 1: Circuit for Question 1.

Consider the circuit depicted in Figure 1. The value v_i of the voltage source is constant. The switch is kept in position **A** for a very long time. At time $t = 0$, it is moved to position **B**.

Q1. Part I: [2 points] Find the initial condition $v_C(0)$ for the capacitor.

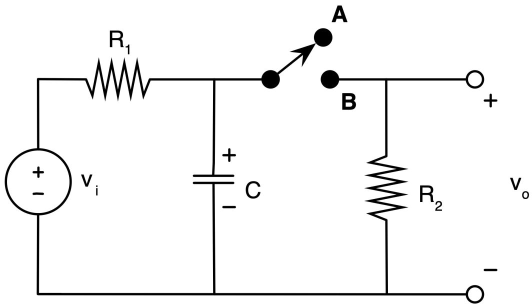

Figure 1: Circuit for Question 1.

Consider the circuit depicted in Figure 1. The value v_i of the voltage source is constant. The switch is kept in position **A** for a very long time. At time $t = 0$, it is moved to position **B**.

Q1. Part II: [2 points] Transform the circuit in Figure 1 into the s-domain, using a current source to account for the initial condition of the capacitor.

Q1. Part III: [2 points] For the circuit you obtained in Part II, find the voltage transform $V_o(s)$. The answer should be given as a ratio of two polynomials.

Q1. Part IV: [2 points] What are the zero-state and zero-input components of $V_o(s)$?

Q1. Part V: [2 points] What are the forced and natural components of $V_o(s)$?

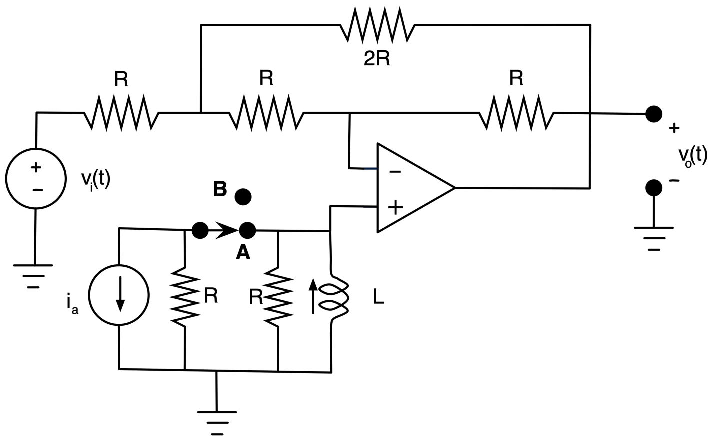

Figure 2: RL circuit for Laplace Analysis for Question 2.

Q2. Part I: [1 point] Consider the circuit depicted in Figure 2. The value i_a of the current source is constant. The switch is kept in position **A** for a very long time. At time $t = 0$, it is moved to position **B**. Find the initial condition for the inductor.

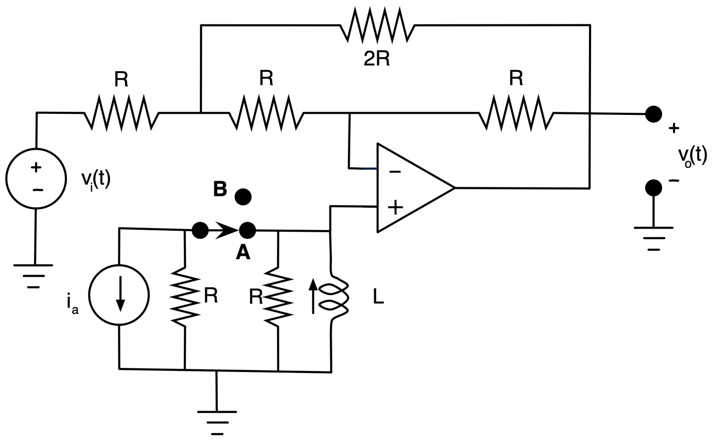

Figure 2: RL circuit for Laplace Analysis for Question 2.

Q2. Part II: [2 points] Use this initial condition to transform the circuit into the s-domain for $t \geq 0$. Use an equivalent model for the inductor in which the initial condition appears as a voltage source.

Q2. Part III: [5 points] Use nodal analysis to show that the output response transform $V_o(s)$ as a function of $V_i(s)$ and i_a is expressed as

$$V_o(s) = -\frac{1}{3}V_i(s) + \frac{4}{3}\frac{RLi_a}{R + sL}$$

Q2. Part IV: [2 points] Use inverse Laplace transforms to show that the output voltage $v_o(t)$ when $v_i(t) = (1 - e^{-t})u(t)\,V$, $L = 1\,\text{mH}$, $i_a = 10\,\text{m}A$, and $R = 100\,\Omega$ is

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Q3. Part I: [2 points] Compute the gain function $|T(j\omega)|$ and the phase function $< T(j\omega)$

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Q3. Part II: [4 points] What are the DC gain and the ∞-freq gain? What are the corresponding values of the phase function? What are the cut-off frequencies?

Q3. Part III: [2 points] Sketch plots for the gain and phase functions. What type of filter is this one?
[Explain your answer]

Q3. Part IV: [2 points] Using what you know about frequency response, compute the steady-state response $v_o^{SS}(t)$ to the input $v_m(t)$. Did the transfer function selected by the engineer accomplish its goal?
[Justify your answer]

In this question, you seek to design a circuit that implements the transfer function

$$T(s) = \frac{10s}{s^2 + 11s + 10}$$

used by the engineer in Question 3 to filter the sensor signal.

Q4. Part I: [2 points] Decompose $T(s)$ as a product $T_1(s) \cdot T_2(s)$ of two transfer functions $T_1(s), T_2(s)$ of the form

$$T_1(s) = \frac{s}{s + \alpha_1}, \quad T_2(s) = \frac{\alpha_2}{s + \alpha_2},$$

with $\alpha_1 < \alpha_2$.

Q4. Part II: [4 points] Design a voltage divider that implements the transfer function $T_1(s)$ and another voltage divider that implements the transfer function $T_2(s)$. You can use only capacitors and resistors, but no inductors. Allowable capacitor values are $10\,\mu$F, $100\,\mu$F, and resistors should be $10\,\mathrm{K}\Omega$.

Q4. Part III: [2 points] Based on the decomposition in Part I and the designs in Part II, the engineer connected in series the two voltage dividers, but was surprised to see that, after filtering the sensor signal $v_m(t)$, the output was not the same as what you computed in Question 3, Part IV. Explain why.

Q4. Part IV: [2 points] How would you fix the design of the engineer in Part III so that the output of the filtered signal is indeed the same as what you computed in Question 3, Part IV? In your design, you can use up to one Op-Amp. Justify your design properly.

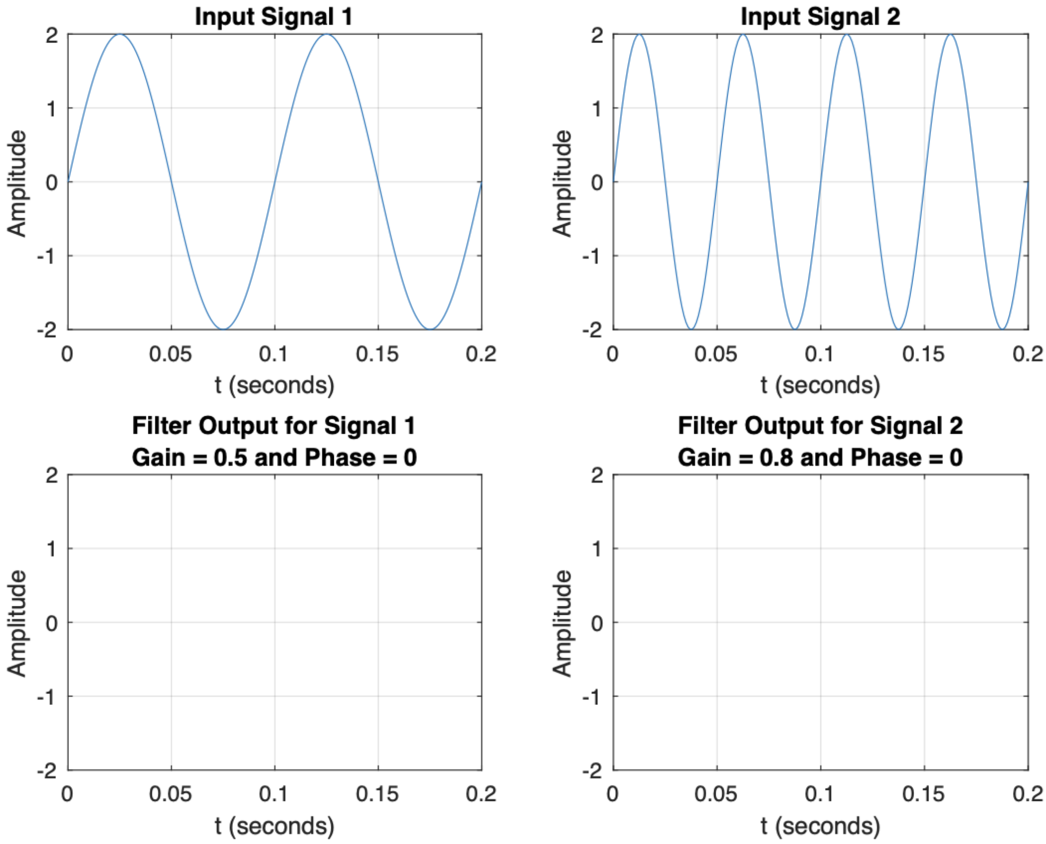

Figure 3: Signals for Question 5.

Figure 3 shows 2 input waveforms that go into a filter.

Q5. Part I: [Extra 1 point] Freehand sketch the filter's steady state output waveform in the time domain using the gain and phase shift shown in the title of the plots. Use the grid lines to draw the output waveform.

Q5. Part II: [Extra 1 point] Is the filter a low-pass filter? Could it be a high-pass filter?

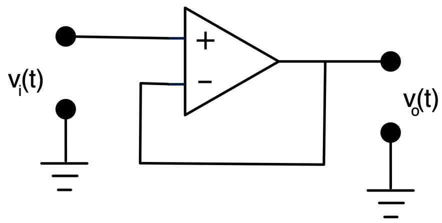

Figure 4: Circuit for Question 6.

For Op-Amp circuit shown in Figure 4, answer the questions below.

Q6. Part I: [Extra 1 point] Calculate v_o as a function of v_i.

Q6. Part II: [Extra 1 point] Explain why someone would use the above circuit in-between two stages instead of just directly connecting the two stages.