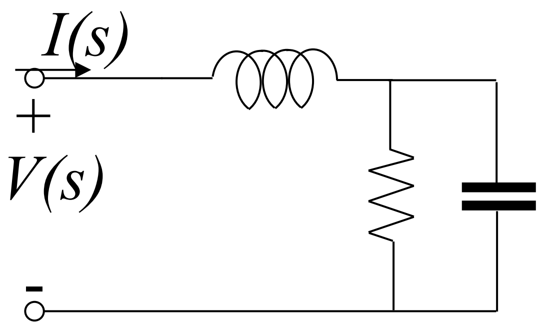
Designing Circuits – Synthesis - Lego

Port = a pair of terminals to a cct

One-port cct; measure I(s) and V(s) at same port

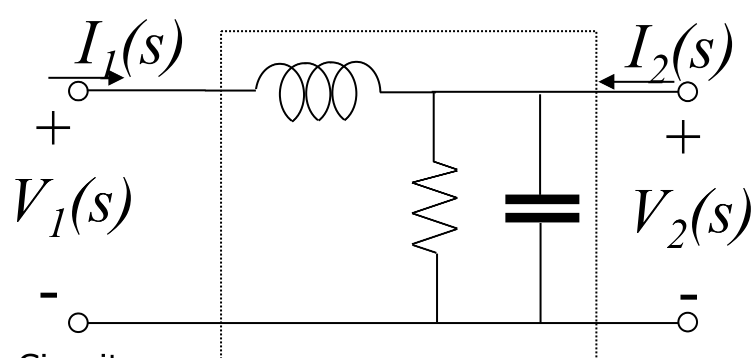


$$Z(s) = \frac{V(s)}{I(s)} = sL + \frac{1}{R^{-1} + sC}$$

Driving-point impedance = input impedance = equiv impedance =Z(s)

Two-ports

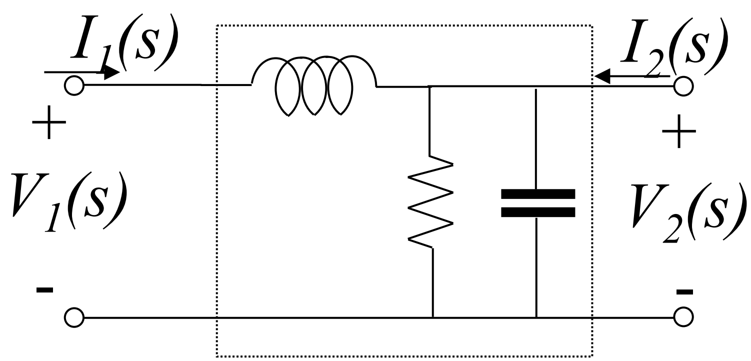
Transfer function; measure input at one port, output at another



Inputs
Outputs

Transfer functions

Transfer function; measure input at one port, output at another

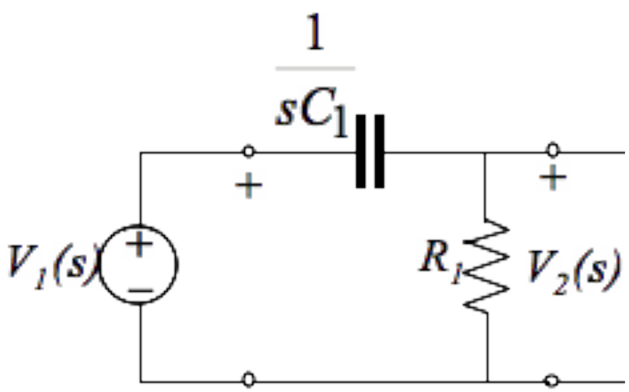


Inputs
Outputs

$$\text{Transfer function} = \frac{\text{zero-state response transform}}{\text{input signal transform}}$$

(I.e., what the circuit does to your input)

Example 11-2, T&R, 6th ed



Transfer function?

Input impedance?

$$T_V(s) = \frac{V_2(s)}{V_1(s)} = \frac{R_1}{R_1 + \frac{1}{sC_1}} = \frac{s}{s + \frac{1}{R_1C_1}}$$

$$Z(s) = \frac{V_1(s)}{I_1(s)} = R_1 + \frac{1}{sC_1}$$

Cascade Connections

We want to apply a chain rule of processing

$$T_V(s) = T_{V1}(s) \times T_{V2}(s) \times T_{V3}(s) \times \ldots \times T_{Vk}(s)$$

When can we do this by cascade connection of OpAmp ccts?

Cascade means output of cct_i is input of cct_{i+1}

This makes the design and analysis much easier

This rule works if stage i+1 does not load stage i

Voltage is not changed because of next stage

Either

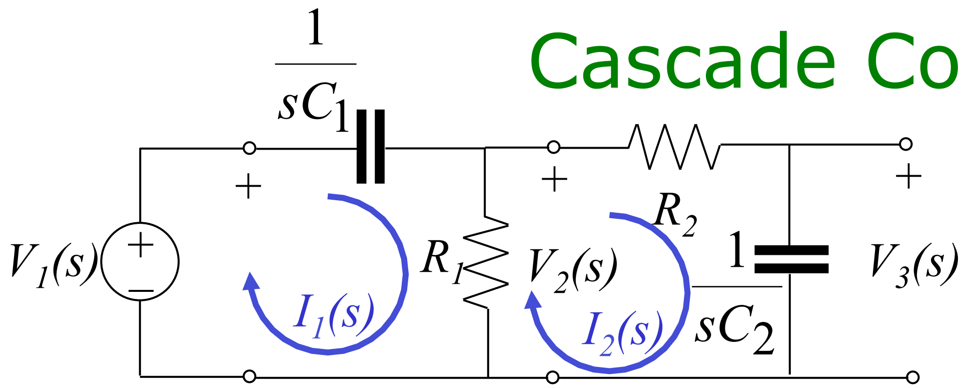
Output impedance of source stage is zero

Or

Input impedance of load stage is infinite

Works well if $Z_{out,source} << Z_{in,load}$

Cascade Connections



Is chain rule valid?

$$T_{Vtotal}(s) \overset{?}{=} T_{V1}(s) \times T_{V2}(s) = \frac{R_1C_1s}{R_1C_1s+1} \times \frac{1}{R_2C_2s+1} = \frac{R_1C_1s}{(R_1R_2C_1C_2)s^2 + (R_1C_1 + R_2C_2)s + 1}$$

Mesh analysis

$$\left(\frac{1}{sC_1} + R_1\right)I_1(s) - R_1I_2(s) = V_1(s)$$

$$-R_1I_1(s) + \left(R_1 + R_2 + \frac{1}{sC_2}\right)I_2(s) = 0$$

$$\begin{pmatrix} I_1(s) \\ I_2(s) \end{pmatrix} = \begin{pmatrix} \frac{1}{sC_1} + R_1 & -R_1 \\ -R_1 & \frac{1}{sC_2} + R_1 + R_2 \end{pmatrix}^{-1} \begin{pmatrix} V_1(s) \\ 0 \end{pmatrix}$$

$$I_2(s) = \frac{s^2C_1C_2R_1}{(R_1R_2C_1C_2)s^2 + (C_1R_1 + C_2R_1 + C_2R_2)s + 1}V_1(s)$$

$$V_3(s) = \frac{1}{sC_2}I_2(s) = \frac{R_1C_1s}{(R_1R_2C_1C_2)s^2 + (R_1C_1 + R_1C_2 + R_2C_2)s + 1}V_1(s)$$

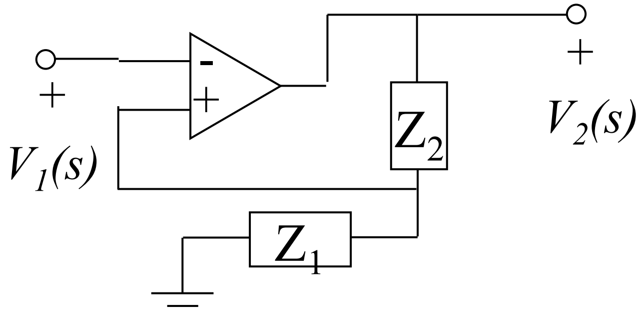
No! Why?

Cascade Connections – OpAmp ccts

OpAmps can be used to achieve the chain rule property for cascade connections

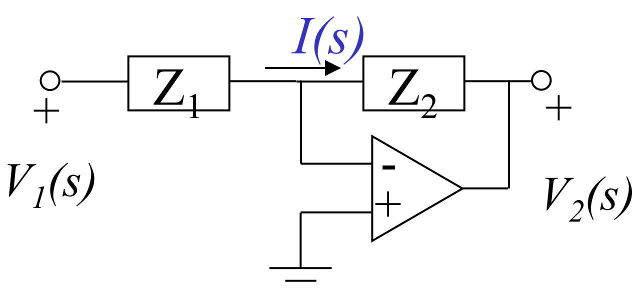
The input to the next stage needs to be driven by the OpAmp output

Consider standard configurations



Noninverting amplifier

No current drawn from V_1 – no load

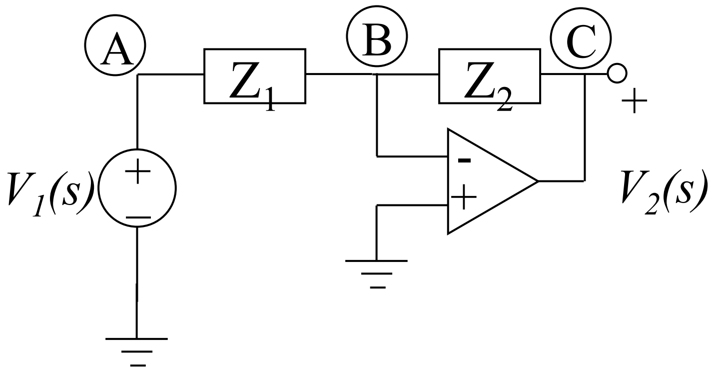


Inverting amplifier

Current provided by $V_1(s)$ $$I(s) = \frac{V_1(s)}{Z_1(s)}$$

Need to make sure that stage is driven by OpAmp output to avoid loading $V_1(s)$

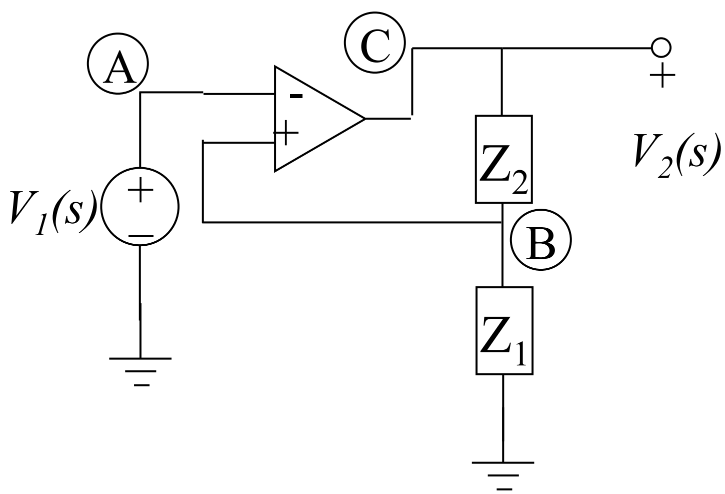
OpAmp Ccts and transfer functions



Node B:

$$\frac{V_B(s)-V_1(s)}{Z_1(s)}+\frac{V_B(s)-V_2(s)}{Z_2(s)}=0$$

$$V_B(s)=0 \quad \Rightarrow T_V(s)=\frac{V_2(s)}{V_1(s)}=-\frac{Z_2(s)}{Z_1(s)}$$



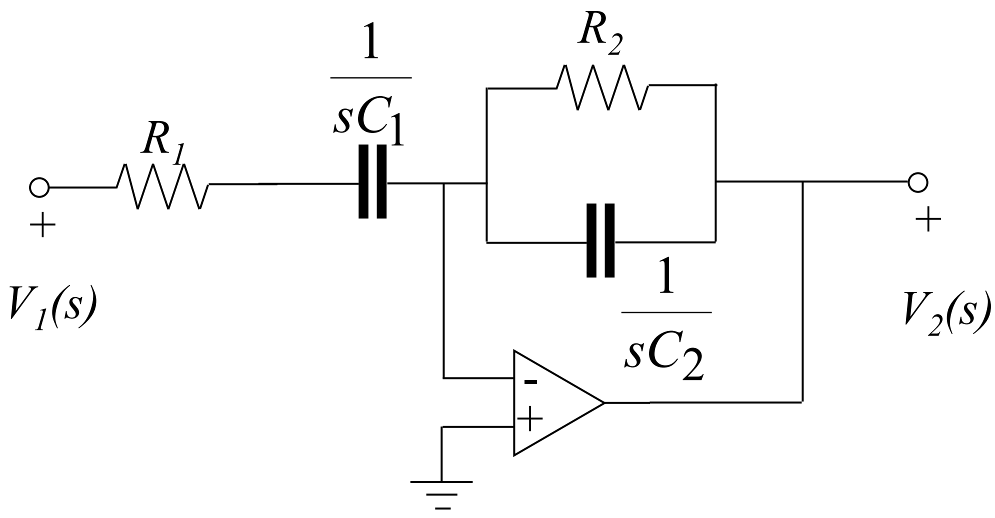
Node B:

$$\frac{V_B(s)-V_2(s)}{Z_2(s)}+\frac{V_B(s)}{Z_1(s)}=0$$

$$V_B(s)=V_1(s) \Rightarrow T_V(s)=\frac{Z_1(s)+Z_2(s)}{Z_1(s)}$$

Example 11-4, T&R, 5th ed, p511

Find the transfer function from $V_1(s)$ to $V_2(s)$



$$Z_1(s) = R_1 + \frac{1}{sC_1} = \frac{sR_1C_1 + 1}{sC_1}$$

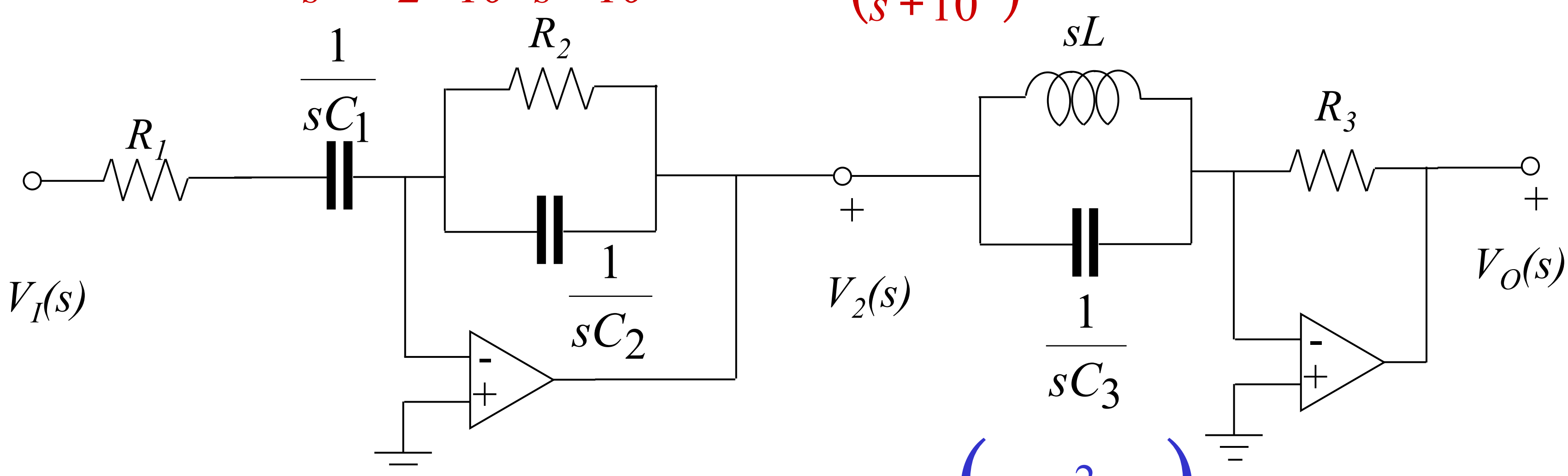
$$Z_2(s) = \frac{R_2 / sC_2}{R_2 + 1/sC_2} = \frac{R_2}{R_2C_2s + 1}$$

$$T_V(s) = -\frac{sR_2C_1}{(sR_1C_1 + 1)(sR_2C_2 + 1)}$$

Circuits as Signal Processors

Design a circuit with transfer function

$$\frac{s^2+1.42\times10^5}{s^2+2\times10^4 s+10^8}=\frac{(s+j\ 408)(s-j\ 408)}{(s+10^4)^2}$$

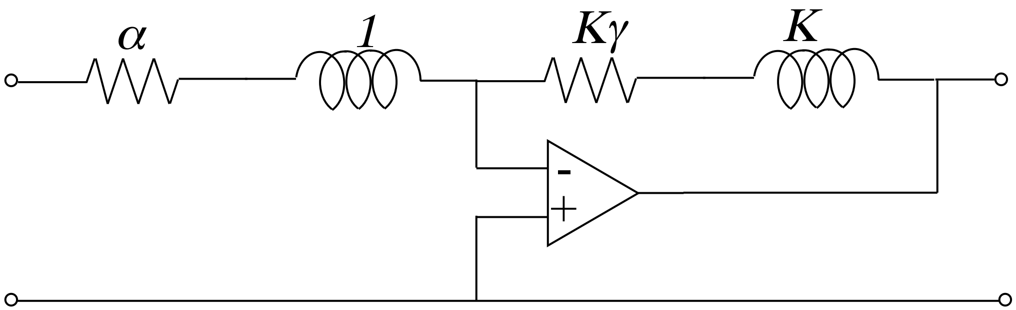


$$T_V(s)=\frac{-sR_2C_1}{(sR_1C_1+1)(sR_2C_2+1)}\times\frac{-R_3\left(LC_3s^2+1\right)}{Ls}$$

$R_1=R_2=100\Omega$, $C_1=C_2=1\mu F$, $C_3=100\mu F$, $L=70mH$, $R_3=1\Omega$

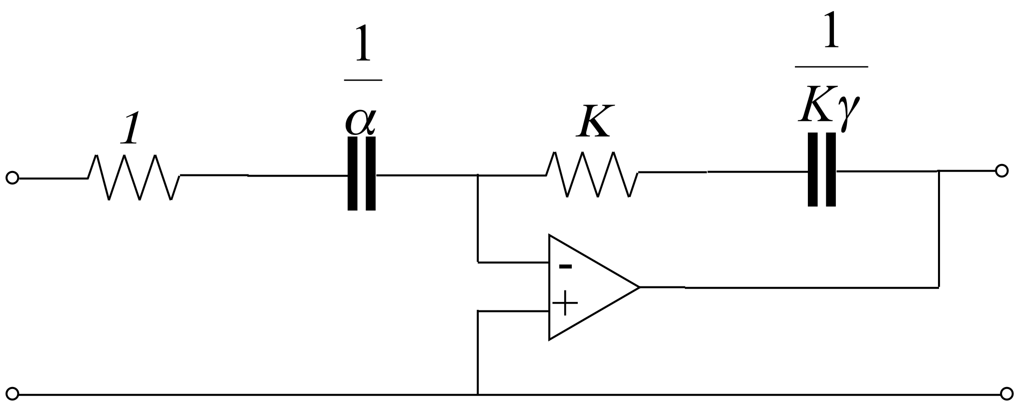
Transfer Function Design – OpAmp Stages

First order stages



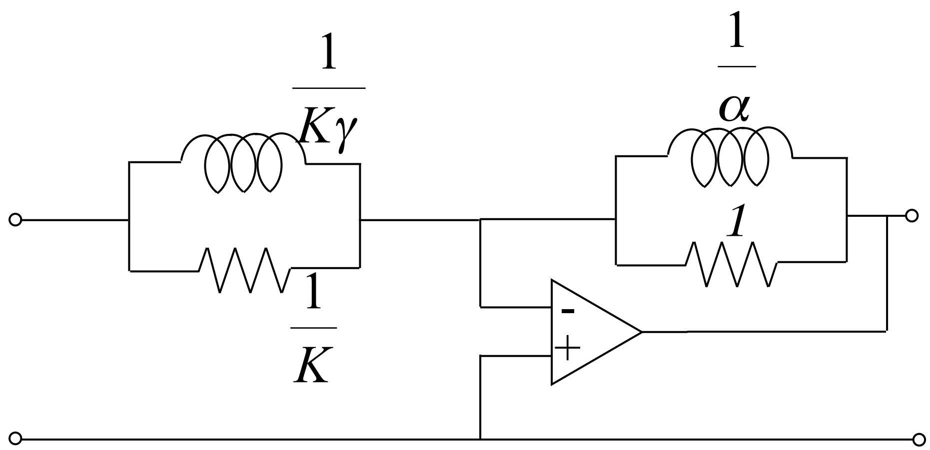
Series RL design

$$T_V(s) = -K\frac{s+\gamma}{s+\alpha}$$

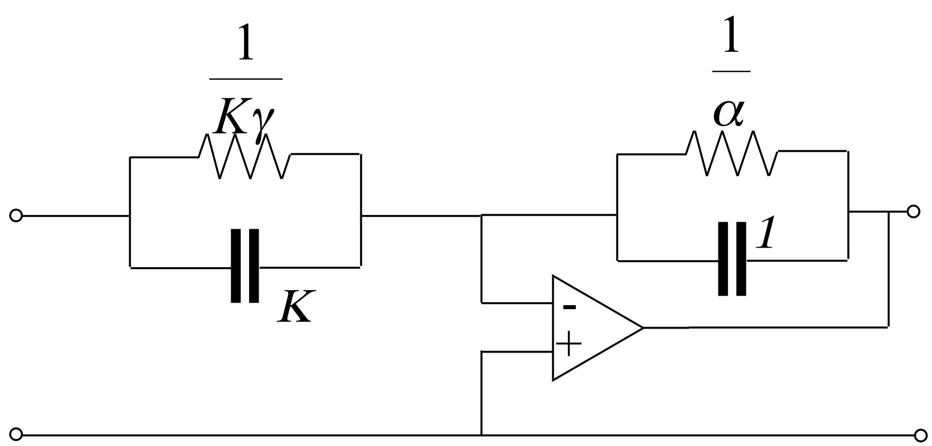


Series RC design

First-order stages



Parallel RL design

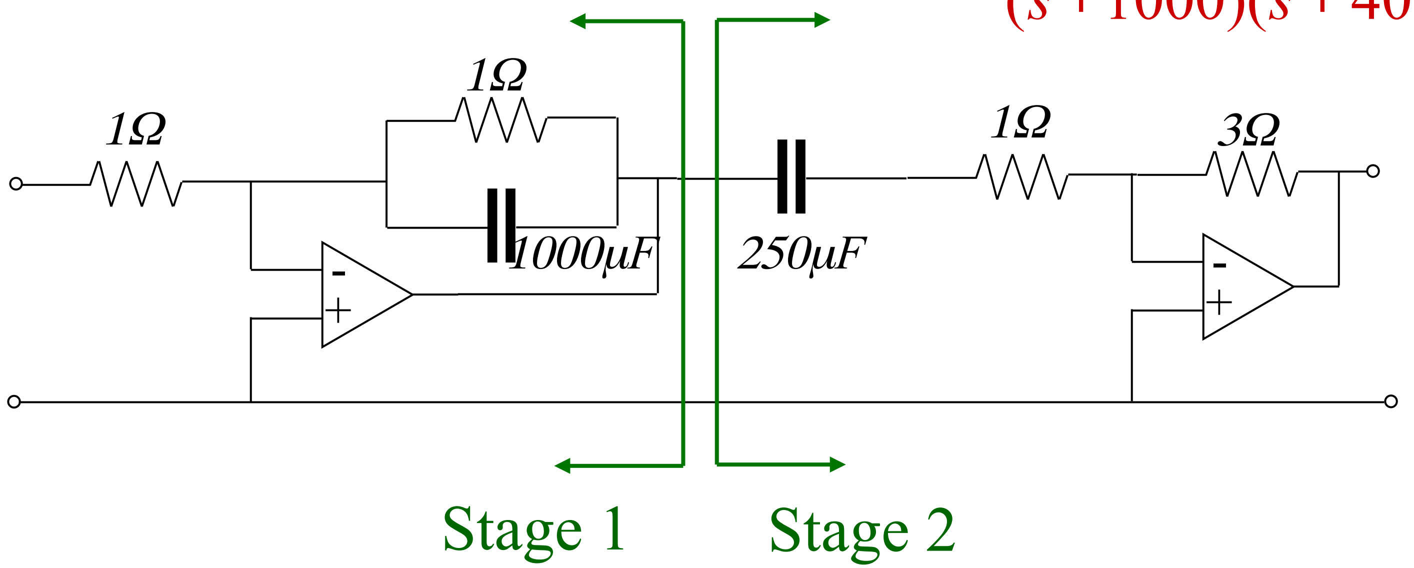


Parallel RC design

$$T_V(s) = -K\frac{s+\gamma}{s+\alpha}$$

Design Example 11-20, T&R, 5th ed, p 542

Design two ccts to realize $T_V(s) = \dfrac{3000s}{(s+1000)(s+4000)}$



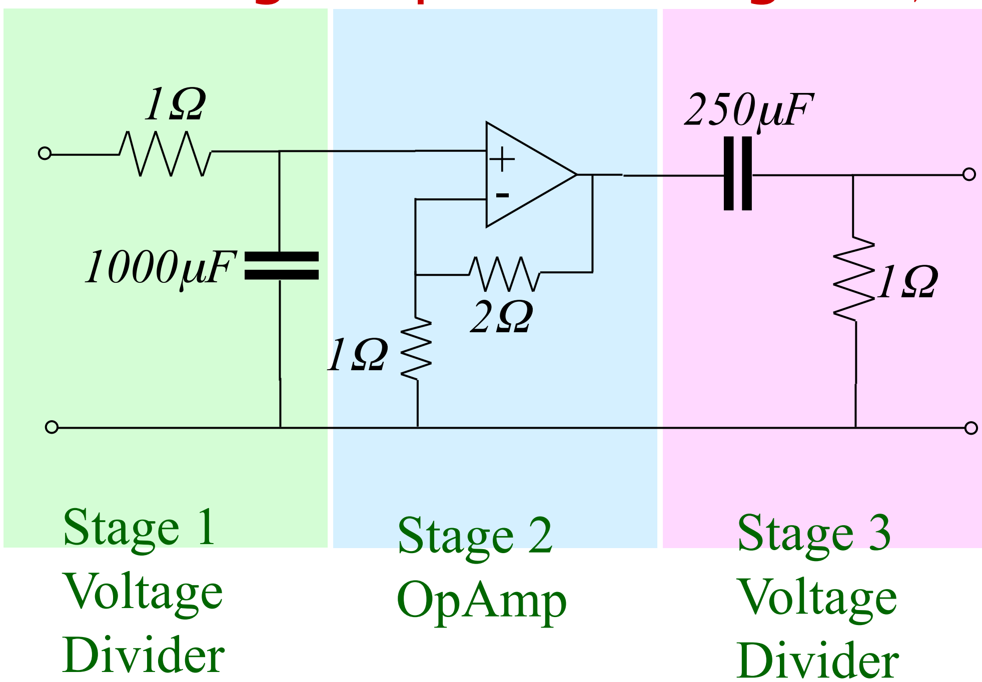
$$T_{V1}(s) = -\left[\frac{1/10^{-3}s}{1+1/10^{-3}s}\right][1]^{-1} = \frac{-1000}{s+1000} \qquad T_{V2}(s) = -[3]\left[1+4000/s\right]^{-1} = \frac{-3s}{s+4000}$$

Unrealistic component values – scaling needed

Design Example 11-19, T&R, 5th ed, p 539

Non-inverting amplifier design

$$T_V(s) = \frac{3000s}{(s+1000)(s+4000)}$$



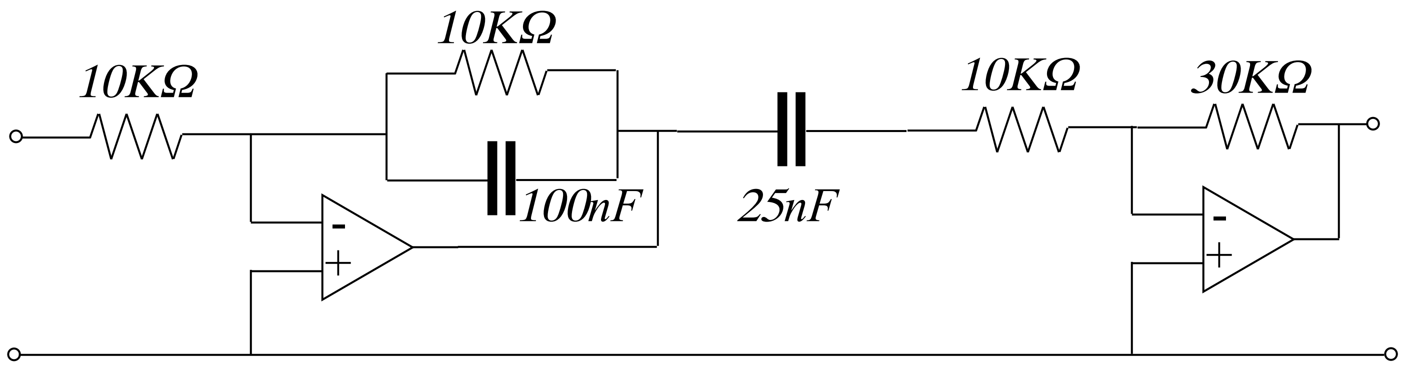
Less OpAmps but more difficult design

Three stage: last stage not driven

Unrealistic component values still – scaling needed

Scaled Design Example 11-21, T&R, 5th ed, p 544

More realistic values for components



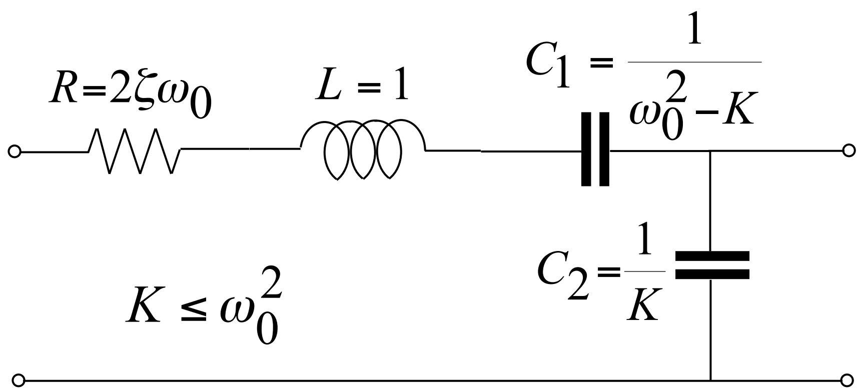
Need to play games with elements to scale

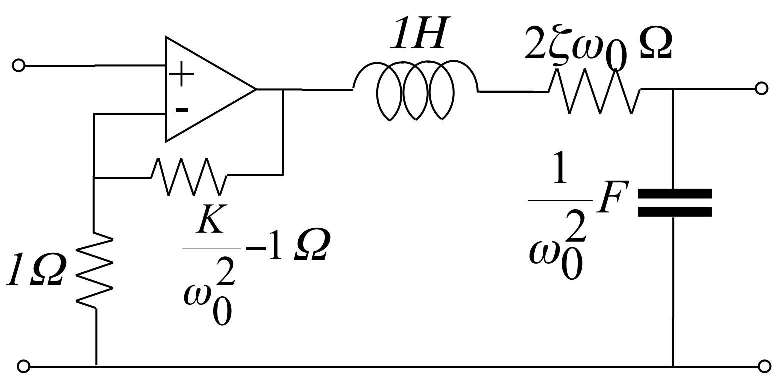
- The ratio formulas for T_V help permit this scaling
  - It certainly is possible to demand a design T_V which is unrealizable with sensible component values
    - Like a pole at 10^{-3} Hz

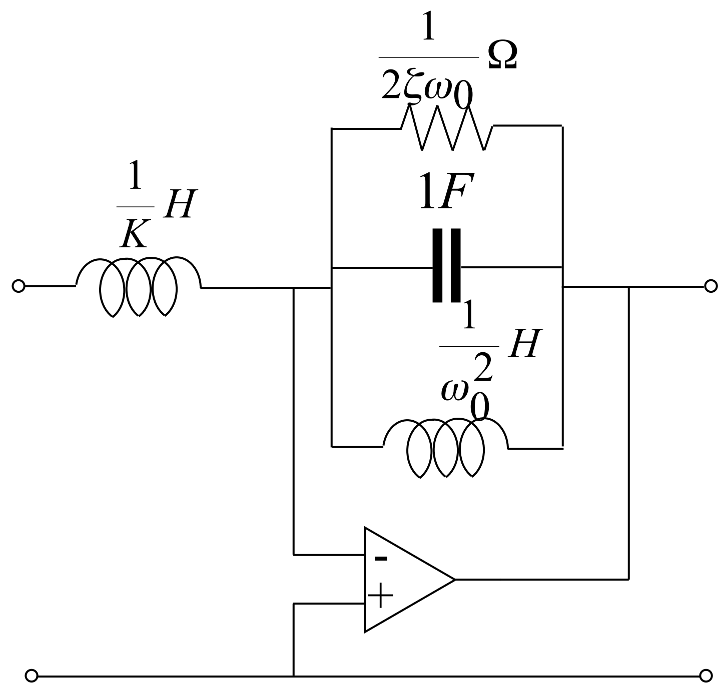
Second-order Stage Design

Circuit stages to yield

$$T_V(s) = \frac{K}{s^2 + 2\varsigma\omega_0 s + \omega_0^2}$$







Circuit Synthesis

Given a stable transfer function $T_V(s)$, realize it via a cct using first-order and second-order stages

$$T_V(s) = \frac{\alpha s^2 + \beta s + \gamma}{as^2 + bs + c} \qquad T_V(s) = \frac{\alpha s + \beta}{as + b}$$

- We are limited to stable transfer functions to keep within the linear range of the OpAmps
  - There is an exception
    - When the unstable $T_V(s)$ is part of a stable feedback system
      - Come to MAE143B to find out

Transistor cct design is conceptually similar