MAE40 - Linear Circuits - Winter 24<br>Final Exam, March 19, 2024

## Instructions

(i) The exam is open book. You may use your class notes and textbook.
(ii) The exam has 4 questions and 1 bonus question, for a total of 40 points and 5 bonus points.
(iii) You have from 8:00am to 11:00am to do the exam - but should require less time!
(iv) You can use a calculator with no communication capabilities.
(v) In your responses, clearly articulate your reasoning and properly justify the steps.
(vi) Important: start each part below on a separate page, use only one side, and write your name \& PID at the top of each page.
Good luck!

## 1. Brief bonus question for extra points



Figure 1: Circuit for Question 1.

Consider the circuit depicted in Figure 1. The value $v_{i}$ of the voltage source is constant. The switch is kept in position $\mathbf{A}$ for a very long time. At time $t=0$, it is moved to position $\mathbf{B}$.

Part I: [Extra 2 points] Find the initial condition $v_{C}(0)$ for the capacitor and $i_{L}(0)$ for the inductor.
Part II [Extra 1 point] Transform the circuit in Figure 1 into the $s$-domain, using current sources to account for the initial conditions.


Figure 2: RL circuit for Laplace Analysis for Question 2.

## 2. Laplace Domain Circuit Analysis

Part I: [2 points] The initial condition of the inductor is $i_{L}(0)=i_{a} A$. Use this initial condition to transform the circuit into the $s$-domain. Use an equivalent model for the inductor in which the initial condition appears as a voltage source.

Part II: [4 points] Use nodal analysis to show that the output response transform $V_{o}(s)$ as a function of $V_{i}(s)$ and $i_{a}$ is expressed as

$$
V_{o}(s)=\frac{3 L\left(R i_{a}+s V_{i}(s)\right)}{2 R+L s}
$$

Part III: [2 points] Use inverse Laplace transforms to show that the output voltage $v_{o}(t)$ when $v_{i}(t)=$ $t u(t) V, L=10 \mathrm{mH}, i_{a}=200 \mathrm{~mA}$, and $R=10 \Omega$ is

$$
v_{o}(t)=\left(\frac{11997}{2000} e^{-2000 t}+\frac{3}{2000}\right) u(t)
$$

Part IV: [2 points] Decompose the output voltage of Part III as (i) the sum of the natural and forced response, and (ii) the sum of the zero-state and zero-input response.

## 3. Basic Building Blocks and Chain Rule



Figure 3: Circuits for Question 3.

We are given the 3 circuits in Figure 3. Two of those circuits are basic op-amp building blocks and one of them is a voltage divider, but we do not know which one is which. All three circuits use resistors of the same value $R$ (so no capacitors, no inductors). We have two tasks: first, identify each circuit by probing with a sinusoidal input signal and, second, use this knowledge to ascertain what would happen to the input signal when we try different combinations in series of these circuits.

Part I: [3 points] When use the signal $x(t)$ in Figure 4(a), you obtain the steady-state outputs depicted in Figure $4(\mathrm{~b}-\mathrm{d})$. With this information, identify each circuit, i.e., is it a voltage divider or a basic op-amp circuit and, in the latter case, which type? In all cases, identify the gain too.
Part II: [2 points] Plot the steady-state response of the connection in series of circuit 1 and circuit 3 (in that order). Does the order in which the circuits are connected matter? Why?

Part III: [2 points] Plot the steady-state response of the connection in series of circuit 2 and circuit 3 (in that order). Does the order in which the circuits are connected matter? Why?
Part IV: [2 points] Plot the steady-state response of the connection in series of circuit 1 and circuit 2 (in that order). Does the order in which the circuits are connected matter? Why?
Part V: [Extra 2 points] Plot the steady-state response of the connection in series of circuit 2, circuit 3, and circuit 1 (in that order).

## 4. Wave Trap and Frequency Response

An engineer faced radio-frequency problems in their recently acquired drone. It turns out the manufacturer had placed the transmitter and radio receiver too close to each other. This resulted in the transmitter


Figure 4: Input and steady-state responses obtained for each circuit.
swamping all signals for the receiver (the signals used by the transmitter were so strong that they overpowered any other signal). Knowing the transmitter used signals with frequencies in the range $250-350 \mathrm{rad} / \mathrm{s}$, instead of returning the drone, the engineer (who had taken MAE40) designed a circuit with transfer function

$$
T(s)=-\frac{10 s^{2}+2000 s+10^{6}}{s^{2}+1100 s+10^{5}}
$$

for the radio receiver, with the intent of greatly reducing the interference from the nearby transmitter. In this problem, you will decide whether this was a reasonable choice. Do the following:

Part I [2 points] Compute the gain function $|T(j \omega)|$ and the phase function $<T(j \omega)$
Part II [4 points] What are the DC gain and the $\infty$-freq gain? What are the corresponding values of the phase function? What are the cut-off frequencies (you can use the information that $T_{\max }=10$ )?
Part III [2 points] Sketch a plot for the gain function. What type of filter is this one?
[Explain your answer]
Part IV [3 points] Using what you know about frequency response, compute the steady-state response $v_{o}^{S S}(t)$ to the inputs $v_{i 1}(t)=A \cos (250 t+\phi), v_{i 2}(t)=A \cos (300 t+\phi)$, and $v_{i 3}(t)=A \cos (350 t+\phi)$. Did the circuit designed by the engineer accomplish its goal?
[Justify your answer]

## 5. Op-amp Circuit Design

In this question, you seek to design a circuit that implements the transfer function

$$
T(s)=-\frac{10 s^{2}+2000 s+10^{6}}{s^{2}+1100 s+10^{5}}
$$

used by the engineer in Question 4.

Part I: [2 points] Decompose $T(s)$ as a sum $T_{1}(s)+T_{2}(s)$ of two transfer functions $T_{1}(s), T_{2}(s)$ of the form

$$
T_{1}(s)=\frac{-K_{1} s}{s+\alpha_{1}}, \quad T_{2}(s)=\frac{-K_{2}}{s+\alpha_{2}}
$$

with $\alpha_{2} \ll \alpha_{1}$ and $K_{1}, K_{2}>0$.
Part II: [4 points] Design a circuit that implements the transfer function $T_{1}(s)$ and another circuit that implements the transfer function $T_{2}(s)$. You can use only capacitors and resistors, but no inductors, and one op-amp per circuit. Allowable capacitor values are $1 \mu \mathrm{~F}, 10 \mu \mathrm{~F}$ and allowable resistor values are $100 \Omega$ and $1 \mathrm{~K} \Omega$.
Part III: [2 points] Based on the decomposition in Part I and the designs in Part II, provide a circuit that implements the transfer function $T(s)$.
Part IV: [2 points] What will be the transfer function corresponding to the connection in series of your two circuits in Part II? Justify your answer. Where is the passband?

